## EXPERIMENT #9

ANALOG TO DIGITAL CONVERTER

As preparation for the laboratory, examine the final circuit diagram at the end of these notes and write a brief plan for the project, including a list of the components needed and a layout of how the circuit will actually be assembled on your circuit board.

In this experiment you will construct an analog to digital converter, making use of several of the principles that you have investigated so far in this course.

Schmitt-trigger Inverter:

The MC54/**74HC14**A Inverters you have been using are a special type of inverter which incorporates **hysteresis** in the input triggering characteristic. In other words, the input voltage level required to cause the output to make a transition from one state to the other **depends** on which state characterizes the output. This characteristic is displayed in the accompanying figure.
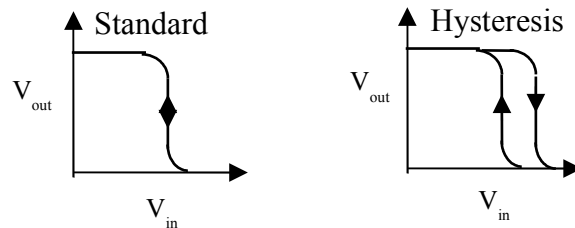
E) Using the output of the D.C. power supply as the input to one of your inverters, measure the two threshold levels of the unit. That is, determine the amount of hysteresis characterizing the device.

The presence of hysteresis of this kind increases the versatility of the unit. In particular, Schmitt-trigger circuits provide excellent noise immunity and the ability to "square up" signals with long rise and fall times. An application of interest to us is the ability to construct a simple "square wave oscillator" from such an inverter.

F) Assemble the following circuit:

kHz Square Wave Oscillator

1 kΩ

0.01 μF
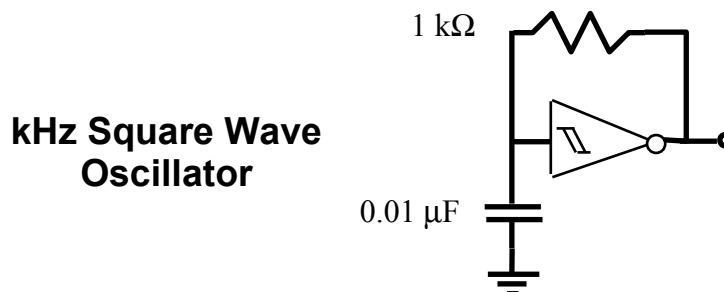
Explain its operation. To explain it you will find it helpful to measure the input voltage and output voltage simultaneously on the oscilloscope.

For your **ADC** (Analog to Digital Converter) which you will be assembling shortly, you will need a "pulse" generator providing "short" pulses every few seconds. This is required in order to trigger the ADC into performing measurements of the input analog signal repetitively, a few times a second.

G) The "short" pulses are generated by the following circuit, when connected to the output of the square wave oscillator.

50 pF

10 kΩ
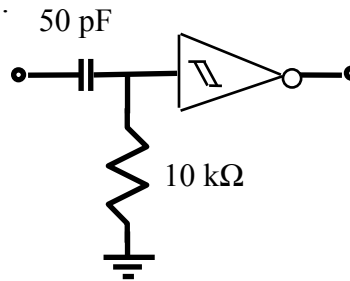
Assemble the circuit shown and connect it to the output of the square wave oscillator.

Verify that the circuit performs the intended function. Explain its operation.

Now decrease the oscillation frequency of your square wave oscillator (part **F**) by first changing the 0.01 µF capacitor to 1.0 µF and then connecting a 220µF capacitor in parallel with it. (Note: Capacitors with **large** values (100's of µF) of capacitance are **electrolytic** capacitors which are polarized. They must be inserted into the circuit with appropriate care. In this case, the negative (**black**) side must be grounded.

 Leave this combination of circuits on your breadboard. They will be incorporated later into your ADC. They will be referred to then as circuit "O1".

H)   For your ADC, you will require another square pulse generator, a unit generating a train of "clock" pulses which when "counted" by a scaler will generate the digital output of the device. Thus, it is now an appropriate time to assemble it onto your breadboard as well.

4.7 kΩ

5 kΩ

Clock Pulse Generator

0.01 µF
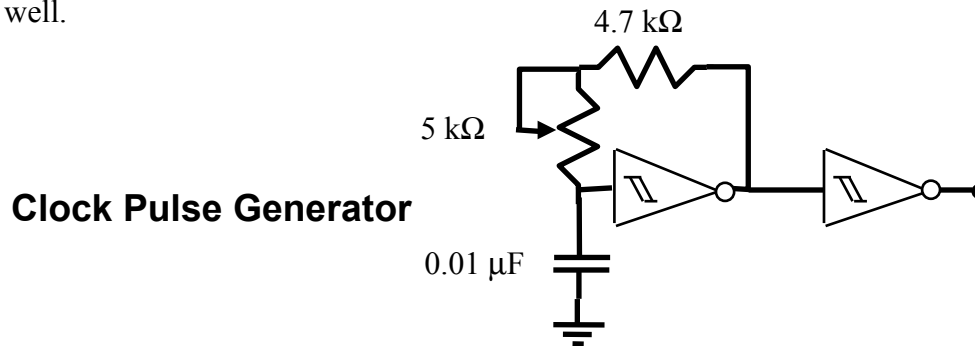
Assemble this circuit and make sure that it produces a square wave with a frequency of ≅ 10 kHz. The 5 kΩ "variable" resistor enables you to tune the frequency of your oscillator over a 2:1 frequency range.

Leave this combination on your breadboard, too. When used in your ADC, it will be referred to as circuit "O2".

I) As shown in the following figure, connect the two decade counters to each other, so that a ÷100 counter is formed.
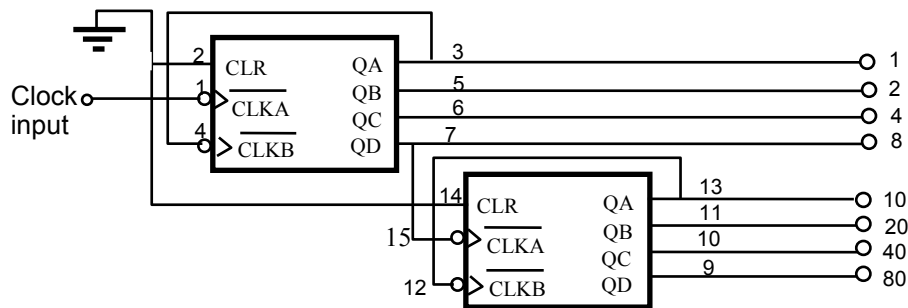
With the ÷100 counter connected to the *7 Segment Decimal Display* devices, verify the operation of this whole counting system, by feeding a **negative** pulse train into the ÷100 counter. You should see the numeric display count in the usual "base-10" fashion.
In order to "reset" the decade counter, the appropriate inputs of the decades (pins 2 and 14) should be connected to a ground potential (or to the second push-button whose output resides at ground to enable you to reset the counter by depressing the button).

Retain this final circuit on your breadboard. It is also required for your ADC.

ANALOGUE TO DIGITAL CONVERTER

Even today, there is still a large body of instrumentation involving analogue signals (voltages and currents). In order to use a computer for monitoring, acquiring or operating on data from such instrumentation, the analogue information must first be converted to digital quantities. The <u>A</u>nalog to <u>D</u>igital <u>C</u>onverter (ADC) accomplishes this task.

There are many techniques utilized by commercial ADC's to perform the A-to-D conversion. One of the simplest methods (and still encountered in practice) involves an Analog to Time Converter. This is a device which, on receipt of an appropriate "trigger" pulse, generates a "stop" pulse at a time t later, where t is **proportional** to the voltage level being digitized.
By gating a free-running "clock" with a pulse whose time duration is equal to t, and counting the gated clock pulses in an appropriate counter (or scaler), the desired analog-to-digital conversion is obtained.
This is the type of ADC which you will assemble in this experiment.

Of the required circuitry:
   1) Analogue to Time Converter
   2) Trigger Generator
   3) Clock
   4) Control Logic
   5) Divide-by-100 Counter and Numeric Display
the Trigger generator (2) is your circuit "O1", the Clock (3), is "O2", the Control logic (4) is your "FF" together with an additional NAND gate, and the Counter and Numeric Display (5) is the **74HC390** Dual 4-Stage Counter connected to the *7 Segment Decimal Display Decoder,* used in Part **L**.

Analog to Time Converter:

 The Analog to Time Converter (1) is the item which we must now address.
It is a circuit which consists of two parts:
i) The first part is a circuit which, on receipt of a "start" pulse (produced by the Trigger circuit), generates a "voltage ramp" (a linearly increasing voltage signal).
ii) The second is a voltage comparator which compares the input (d.c.) voltage signal whose value is to be determined, with this voltage ramp **(i)**, generating an output pulse, the "stop" signal, when the ramp exceeds the input.

As well as resetting the ramp generator back to it quiescent state, this "stop" pulse also resets the control circuit flip-flop, thus cutting off the clock pulses from the decade counter.
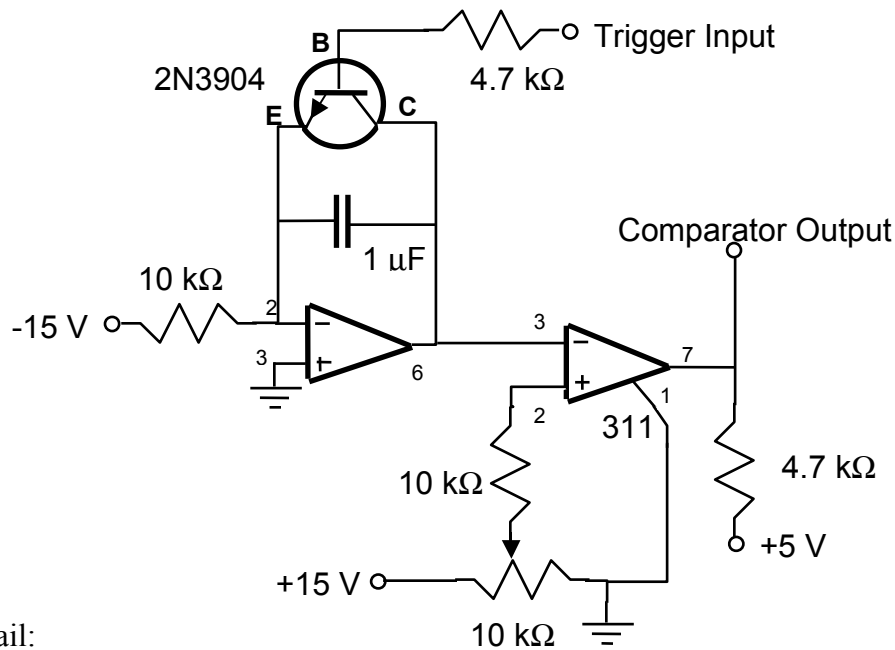
In detail:

i) The voltage ramp circuit is an op-amp current integrator. Its input is a 1.5 mA DC constant current (15 V $\div$ 10 kΩ), which when integrated on the 1 µF feedback capacitor (C5), yields a positive ramp voltage output signal. The transistor in parallel with the feedback capacitor is an electronic switch controlled by the logic circuit. When "open" (resulting when a Lo level is applied to its input), the integrator operates in the fashion described, producing the required ramp voltage at its output. However, when the switch is "closed" (resulting when a Hi level is applied to its input), the feedback capacitor is shorted out, and, since the 1.5 mA current flowing through the switch results in an insignificant potential drop, a "zero" (Lo) voltage is produced at the output of the **741** OpAmp.

ii) The comparator is a second op-amp (type **311** difference amplifier). This comparator is related to the op-amp you studied in experiment 5, but differs from the usual type of OpAmp (like the **741)** in that it is very fast, has a large input resistance, yet is still cheap. Further, it is designed so that it can be coupled to "almost anything". In this circuit it yields an upper or lower voltage level (+5V or GND) depending on whether the value of the ramp voltage is less than or greater than the input voltage set by the potentiometer R6. Operationally, as the ramp voltage moves past the input voltage level, the output of the comparator makes a sudden transition from Hi to Lo.

M) Construct the Ramp Generator (with transistor switch) and Comparator circuit using the **741** OpAmp, **2N3904** transistor and **311** Voltage Comparator supplied with your unit. Refer to the pin connections shown on the data sheets for the OpAmp and Comparator to determine where to connect the required +15V and -15V power. **Notice that these pin connections are different for the two devices!**

The input d.c. voltage signal is derived from the 10 kΩ (blue) potentiometer (R6) provided on the breadboard.

An important note: Pin 1 of the 311 comparator must be connected to ground in order for the comparator to function properly.

To test the circuit, adjust the potentiometer so that a d.c. input voltage level intermediate between GND and +15V is provided to the **311**, and apply a square wave signal (Hi to Lo to Hi) to the input of the transistor switch (marked "Trigger Input" in the diagram). Your "kHz Square Wave Oscillator" (circuit "O1") will provide the requisite signal. For this test application, use the circuit of part **F)**, prior to the addition of the short pulse generator of part **G)**, **and with the 220 μF capacitor of part H) temporarily disconnected.** The duration of these square pulses should be long enough for the value of the ramp to exceed the input d.c. signal level before the Lo to Hi transition of the square wave Trigger Input occurs. If this is not the case, decrease the d.c. signal level somewhat so that the ramp can attain the required value quicker. At the instant the ramp exceeds the d.c. signal level, the output of the Comparator will be observed to switch from a Hi level to a Lo level. It then switches back to Hi when the ramp is turned off by the Trigger Input square wave returning from Lo to Hi.

<u>Caution</u>: Do not proceed further until you are sure that the output of the comparator varies between the Hi and Lo logic levels as described. If you fail to follow this advice and proceed to the next section (**N**) with an improperly functioning comparator, you may destroy some of the CMOS devices which will be connected to it!

When you have satisfied yourself that this part of the ADC is working correctly, **reconnect the 220 μF capacitor into the square wave oscillator circuit ("O1").**

You are now ready for the most exciting part of this whole operation!

N) **Assemble the whole ADC circuit,** by inserting two more inverters, and inter-
   connecting your various sub-components according to the following circuit diagram.
   Carefully **recheck** that **all** required interconnections have been incorporated before
   proceeding further!

Mode of Operation:

The trigger generator (circuit "O1") is the device which determines the frequency at
which your d.c. input signal is sampled. Its **short (**negative going) output is used to:
i) Clear the decade counter. But since the decade counter requires a **positive** reset (CLR)
pulse, an additional digital inverter (which also feeds the TP1 test point) is incorporated
between the circuit "01" and the decade counter.
ii) "Sets" the control flip-flop (circuit "FF") which in turn
　　　　opens a gate to allow the clock pulses (from circuit "O2") to pass to the decade
counter. Since **negative-going** signals are required to "set" the FF, the necessary signal
could have been obtained directly at the output of the "01" circuit. However, in order to
be certain that no gated clock pulses can arrive at the decade counter **before** the counter
has been cleared, a slight time delay is provided by using a further inverter following the
TP1 test point. This inverter changes the short **positive** output pulse at TP1 back to the
short negative pulse required to "set" the FF.
　　　　In addition, the control flip-flop opens the electronic (transistor) switch on the
ramp generator to initiate the analogue-to-time conversion process.

Once the ramp voltage reaches the level set by the d.c. input voltage, the negative
transition at the output of the **311** comparator "Resets" the flip-flop which in turn
　　　　closes the gate at the output of the clock, thus preventing any more clock pulses
from reaching the counter, and also
　　　　closes the electronic (transistor) switch which in turn "shorts" the 1 μF
integrating capacitor, thus terminating the production of the ramp and returning the
output level of the integrating **741** OpAmp to ground. At this instant, the **311** comparator
responds by changing its output to a Hi value. Since this whole process which occurs
after the ramp voltage reaches the level set by the d.c. input level takes such a short time,
the duration of the negative output pulse from the comparator is correspondingly short as
well.

The whole cycle is then repeated when the next trigger pulse occurs.

O) Turn on the power, cross your fingers and check whether your circuit operates
   according to expectation. If not, try to determine which subsection is not performing
   properly, and then disconnect it from the circuit and test it by itself.

When things appear to be behaving properly, measure the d.c. voltage level of the input signal and then vary the clock frequency by adjusting the 5kΩ variable resistor in the clock circuit ("O2") so that the decade counter displays the "correct" value of the input voltage (it is sensible to arrange for a reading of 100 to refer to a level of 10 V).

P) Finally, produce a timing diagram for the A-D converter by sketching in your lab book the shapes of the waveforms at various test points that illustrate how different parts of the A-D interact with one another.
*Note: To see the wave forms more clearly, speed up the trigger rate by removing the 220 μF capacitor from the circuit "01". At the same time, you will have to set the value of the d.c. input voltage **low** enough that the ramp voltage is able to reach that value within the timing period set by the trigger oscillator!*