

Today's plan:

- Announcements:
 - Test 1 20 minutes
 - Lab issues
 - Projects
- Lab 5/6:
- Activity 3
- Python and GUI's.
- Timers on the MSP430
- Sensors [next time in detail]
-

Lab issues

Burning ports!

- Inputs should be protected by 330 Ω 1k Ω
- Outputs can not be connected directly to voltage sources or ground.
- Only integers can be send to registers.
- R registers are 16 bits I/O control registers are 8 bits! .b are 8 bits commands, .w are 16 bits
- No arithmetic's on registers

Activity 3 Due on canvas before next lecture

Find the values of x after each of the following C commands (run on an MSP430). Answer in hexadecimal.

unsigned int x = 6;

a) x %= 4;

b) x = 96 >> 2;

c) x = ~65280; Hint: 65280 = 0xFF00

d) x = 32769 << 4; Hint: 32769 = 0x8001

2) Write the lines of C code needed to:

a) set P1.0 to P1.3 to be outputs and P1.4 to P1.7 to be inputs

b) starts a for loop that continuously copies the values on the inputs to the values of the outputs (ie P1.4 -> P1.0, P1.5 -> P1.1 etc).

c) if all four of the inputs are 0, exit the loop.

Using peripherals

```
#include "msp430.h"
```

```
void main(void)
```

```
{
```

```
WDTCTL = WDTPW + WDTHOLD;
```

```
// Stop WDT
```

```
ADC10CTL0 = ADC10SHT_2 + ADC10ON;
```

```
// ADC10ON
```

```
ADC10CTL1 = INCH_1;
```

```
// input A1
```

```
ADC10AE0 |= 0x02;
```

```
// PA.1 ADC option select
```

```
P1DIR |= 0x01 ;
```

```
// Set P1.0 to output
```

```
for (;;)
{
```

```
ADC10CTL0 |= ENC + ADC10SC;
```

```
// Sampling and conversion start
```

```
while (ADC10CTL1 & ADC10BUSY);
```

```
// ADC10BUSY?
```

```
if (ADC10MEM < 0x2FF)
```

```
    P1OUT &= ~0x01;
```

```
// Clear P1.0 LED off
```

```
else
```

```
    P1OUT |= 0x01;
```

```
// Set P1.0 LED on
```

```
unsigned i;
```

```
for (i = 0xFFFF; i > 0; i--);
```

```
// Delay
```

```
}
```

```
}
```

ADC10CTL0 = ADC10SHT_2 + ADC10ON;

// ADC10ON

22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
SREFx			ADC10SHTx		ADC10SR	REFOUT	REFBURST
rw-(0)		rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
MSC	REF2_5V	REFON	ADC10ON	ADC10IE	ADC10IFG	ENC	ADC10SC
Can be modified only when ENC = 0							

SREFx	Bits 15-13	Select reference. 000 $V_{Rn} = V_{CC}$ and $V_{Rl} = V_{SS}$ 001 $V_{Rn} = V_{REF+}$ and $V_{Rl} = V_{SS}$ 010 $V_{Rn} = V_{REF+}$ and $V_{Rl} = V_{SS}$. Devices with V_{REF+} only. 011 $V_{Rn} =$ Buffered V_{REF+} and $V_{Rl} = V_{SS}$. Devices with V_{REF+} pin only. 100 $V_{Rn} = V_{CC}$ and $V_{Rl} = V_{REF-}/V_{REF+}$. Devices with V_{REF-} pin only. 101 $V_{Rn} = V_{REF+}$ and $V_{Rl} = V_{REF-}/V_{REF+}$. Devices with V_{REF+} pins only. 110 $V_{Rn} = V_{REF+}$ and $V_{Rl} = V_{REF-}/V_{REF+}$. Devices with V_{REF+} pins only. 111 $V_{Rn} =$ Buffered V_{REF+} and $V_{Rl} = V_{REF-}/V_{REF+}$. Devices with V_{REF+} pins only.
ADC10SHTx	Bits 12-11	ADC10 sample-and-hold time 00 $4 \times$ ADC10CLKs 01 $8 \times$ ADC10CLKs 10 $16 \times$ ADC10CLKs 11 $64 \times$ ADC10CLKs
ADC10SR	Bit 10	ADC10 sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate. Setting ADC10SR reduces the current consumption of the reference buffer. 0 Reference buffer supports up to ~ 200 ksp/s 1 Reference buffer supports up to ~ 50 ksp/s
REFOUT	Bit 9	Reference output 0 Reference output off 1 Reference output on. Devices with V_{REF+}/V_{REF-} pin only.
REFBURST	Bit 8	Reference burst. 0 Reference buffer on continuously 1 Reference buffer on only during sample-and-conversion
MSC	Bit 7	Multiple sample and conversion. Valid only for sequence or repeated modes. 0 The sampling requires a rising edge of the SHI signal to trigger each sample-and-conversion. 1 The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed
REF2_5V	Bit 6	Reference-generator voltage. REFON must also be set. 0 1.5 V 1 2.5 V
REFON	Bit 5	Reference generator on 0 Reference off 1 Reference on
ADC10ON	Bit 4	ADC10 on 0 ADC10 off 1 ADC10 on
ADC10IE	Bit 3	ADC10 interrupt enable 0 Interrupt disabled 1 Interrupt enabled

ADC10 Registers

ADC10IFG	Bit 2	ADC10 interrupt flag. This bit is set if ADC10MEM is loaded with a conversion result. It is automatically reset when the interrupt request is accepted, or it may be reset by software. When using the DTC this flag is set when a block of transfers is completed. 0 No interrupt pending 1 Interrupt pending
ENC	Bit 1	Enable conversion 0 ADC10 disabled 1 ADC10 enabled
ADC10SC	Bit 0	Start conversion. Software-controlled sample-and-conversion start. ADC10SC and ENC may be set together with one instruction. ADC10SC is reset automatically. 0 No sample-and-conversion start 1 Start sample-and-conversion

ADC10CTL0 = ADC10SHT_2 + ADC10ON;

// ADC10ON

22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
SREFx		ADC10SHTx			ADC10SR	REFOUT	REFBURST
rw-(0)		rw-(0)			rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
MSC	REF2_5V	REFON	ADC10ON	ADC10IE	ADC10IFG	ENC	ADC10SC
Can be modified only when ENC = 0							

SREFx	Bits 15-13	Select reference. 000 $V_{R1} = V_{CC}$ and $V_{R1} = V_{SS}$ 001 $V_{R1} = V_{REF+}$ and $V_{R1} = V_{SS}$ 010 $V_{R1} = V_{REF+}$ and $V_{R1} = V_{SS}$. Devices with V_{REF+} pin only. 011 $V_{R1} =$ Buffered V_{REF+} and $V_{R1} = V_{SS}$. Devices with V_{REF+} pin only. 100 $V_{R1} = V_{CC}$ and $V_{R1} = V_{REF-}/V_{REF-}$. Devices with V_{REF-} pin only. 101 $V_{R1} = V_{REF+}$ and $V_{R1} = V_{REF-}/V_{REF-}$. Devices with V_{REF-} pins only. 110 $V_{R1} = V_{REF+}$ and $V_{R1} = V_{REF-}/V_{REF-}$. Devices with V_{REF-} pins only. 111 $V_{R1} =$ Buffered V_{REF+} and $V_{R1} = V_{REF-}/V_{REF-}$. Devices with V_{REF-} pins only.
ADC10SHTx	Bits 12-11	ADC10 sample-and-hold time 00 $4 \times$ ADC10CLKs 01 $8 \times$ ADC10CLKs 10 $16 \times$ ADC10CLKs 11 $31 \times$ ADC10CLKs
ADC10SR	Bit 10	ADC10 sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate. Setting ADC10SR reduces the current consumption of the reference buffer. 0 Reference buffer supports up to ~ 200 ksp/s 1 Reference buffer supports up to ~ 50 ksp/s
REFOUT	Bit 9	Reference output 0 Reference output off 1 Reference output on. Devices with V_{REF+}/V_{REF-} pin only.
REFBURST	Bit 8	Reference burst. 0 Reference buffer on continuously 1 Reference buffer on only during sample-and-conversion
MSC	Bit 7	Multiple sample and conversion. Valid only for sequence or repeated modes. 0 The sampling requires a rising edge of the SHI signal to trigger each sample-and-conversion. 1 The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed
REF2_5V	Bit 6	Reference-generator voltage. REFON must also be set. 0 1.5 V 1 2.5 V
REFON	Bit 5	Reference generator on 0 Reference off 1 Reference on
ADC10ON	Bit 4	ADC10 on 0 ADC10 off 1 ADC10 on
ADC10IE	Bit 3	ADC10 interrupt enable 0 Interrupt disabled 1 Interrupt enabled

If the register descriptions don't have enough information then:

- 1) Look back earlier in the ADC10 chapter for more description of the operation.
- 2) Check the text book for an alternative description.
- 3) Ask a classmate or one of us!

ADC10IFG	Bit 2	ADC10 interrupt flag. This bit is set if ADC10MEM is loaded with a conversion result. It is automatically reset when the interrupt request is accepted, or it may be reset by software. When using the DTC this flag is set when a block of transfers is completed. 0 No interrupt pending 1 Interrupt pending
ENC	Bit 1	Enable conversion 0 ADC10 disabled 1 ADC10 enabled
ADC10SC	Bit 0	Start conversion. Software-controlled sample-and-conversion start. ADC10SC and ENC may be set together with one instruction. ADC10SC is reset automatically. 0 No sample-and-conversion start 1 Start sample-and-conversion

Using peripherals

```
#include "msp430.h"
```

```
void main(void)
```

```
{
```

```
    WDTCTL = WDTPW + WDTHOLD;
```

```
    // Stop WDT
```

```
    ADC10CTL0 = ADC10SHT_2 + ADC10ON;
```

```
    // ADC10ON
```

```
    ADC10CTL1 = INCH_1;
```

```
    // input A1 (P1.1)
```

```
    ADC10AE0 |= 0x02;
```

```
    // PA.1 ADC option select
```

```
    P1DIR |= 0x01 ;
```

```
    // Set P1.0 to output direction
```

```
for (;;)
{
```

```
    ADC10CTL0 |= ENC + ADC10SC;
```

```
    // Sampling and conversion start
```

```
    while (ADC10CTL1 & ADC10BUSY);
```

```
    // ADC10BUSY?
```

```
    if (ADC10MEM < 0x2FF)
```

```
        P1OUT &= ~0x01;
```

```
    // Clear P1.0 LED off
```

```
    else
```

```
        P1OUT |= 0x01;
```

```
    // Set P1.0 LED on
```

```
    unsigned i;
```

```
    for (i = 0xFFFF; i > 0; i--);
```

```
    // Delay
```

```
}
```

```
}
```

ADC10CTL1 = INCH_1;

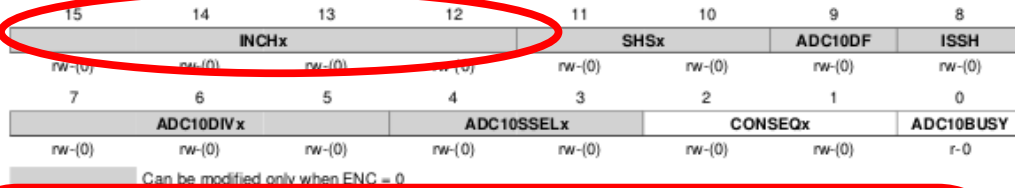
// input A1



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ADC10 Registers

22.3.2 ADC10CTL1, ADC10 Control Register 1



INCHx	Bits 15-12	Input channel select. These bits select the channel for a single-conversion or the highest channel for a sequence of conversions. Only available ADC channels should be selected. See device specific datasheet.
		0000 A0
		0001 A1
		0010 A2
		0011 A3
		0100 A4
		0101 A5
		0110 A6
		0111 A7
		1000 V_{REF+}
		1001 V_{REF+}/V_{REF-}
		1010 Temperature sensor
		1011 $(V_{CC} - V_{SS}) / 2$
		1100 $(V_{CC} - V_{SS}) / 2$, A12 on MSP430F22xx devices
		1101 $(V_{CC} - V_{SS}) / 2$, A13 on MSP430F22xx devices
		1110 $(V_{CC} - V_{SS}) / 2$, A14 on MSP430F22xx devices
		1111 $(V_{CC} - V_{SS}) / 2$, A15 on MSP430F22xx devices
		00 ADC10SC bit
		01 Timer_A.OUT1 ⁽¹⁾
		10 Timer_A.OUT0 ⁽¹⁾
		11 Timer_A.OUT2 (Timer_A.OUT1 on MSP430F20x0, MSP430G2x31, and MSP430G2x30 devices) ⁽¹⁾
ADC10DF	Bit 9	ADC10 data format
		0 Straight binary
		1 2s complement
ISSH	Bit 8	Invert signal sample-and-hold
		0 The sample-input signal is not inverted.
		1 The sample-input signal is inverted.
ADC10DIVx	Bits 7-5	ADC10 clock divider
		000 /1
		001 /2
		010 /3
		011 /4
		100 /5
		101 /6
		110 /7
		111 /8
ADC10SSELx	Bits 4-3	ADC10 clock source select
		00 ADC10OSC
		01 ACLK
		10 MCLK
		11 SMCLK

ADC10 Registers

CONSEQx	Bits 2-1	Conversion sequence mode select
		00 Single-channel-single-conversion
		01 Sequence-of-channels
		10 Repeat-single-channel
		11 Repeat-sequence-of-channels
ADC10BUSY	Bit 0	ADC10 busy. This bit indicates an active sample or conversion operation
		0 No operation is active.
		1 A sequence, sample, or conversion is active.

⁽¹⁾ Timer triggers are from Timer0_Ax if more than one timer module exists on the device.

ADC10CTL1 = INCH_1;

// input A1



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ADC10 Registers

22.3.2 ADC10CTL1, ADC10 Control Register 1

15	14	13	12	11	10	9	8
INCHx				SHSx	ADC10DF	ISSH	
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC10DIVx		ADC10SSELx		CONSEQx		ADC10BUSY	
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0

Can be modified only when ENC = 0

INCHx	Bits 15-12	Input channel select. These bits select the channel for a single-conversion or the highest channel for a sequence of conversions. Only available ADC channels should be selected. See device specific datasheet.
	0000	A0
	0001	A1
	0010	A2
	0011	A3
	0100	A4
	0101	A5
	0110	A6
	0111	A7
	1000	V _{REF+}
	1001	V _{REF-} /V _{REFP}
	1010	Temperature sensor
	1011	(V _{CC} - V _{SS}) / 2
	1100	(V _{CC} - V _{SS}) / 2, A12 on MSP430F22xx devices
	1101	(V _{CC} - V _{SS}) / 2, A13 on MSP430F22xx devices
	1110	(V _{CC} - V _{SS}) / 2, A14 on MSP430F22xx devices
	1111	(V _{CC} - V _{SS}) / 2, A15 on MSP430F22xx devices
	00	ADC10SC bit
	01	Timer_A.OUT1 ⁽¹⁾
	10	Timer_A.OUT0 ⁽¹⁾
	11	Timer_A.OUT2 (Timer_A.OUT1 on MSP430F20x0, MSP430G2x31, and MSP430G2x30 devices) ⁽¹⁾
ADC10DF	Bit 9	ADC10 data format
	0	Straight binary
	1	2s complement
ISSH	Bit 8	Invert signal sample-and-hold
	0	The sample-input signal is not inverted.
	1	The sample-input signal is inverted.
ADC10DIVx	Bits 7-5	ADC10 clock divider
	000	/1
	001	/2
	010	/3
	011	/4
	100	/5
	101	/6
	110	/7
	111	/8
ADC10SSELx	Bits 4-3	ADC10 clock source select
	00	ADC10OSC
	01	ACLK
	10	MCLK
	11	SMCLK

⁽¹⁾ Timer triggers are from Timer0_Ax if more than one timer module exists on the device.

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Table 2. Terminal Functions

NAME	NO.		I/O	DESCRIPTION
	14 N, PW	16 RSA		
P1.0/ TA0CLK/ ACLK/ A0	2	1	I/O	General-purpose digital I/O pin Timer0_A, clock signal TACLK input ACLK signal output ADC10 analog input A0 ⁽¹⁾
P1.1/ TA0.0/ A1	3	2	I/O	General-purpose digital I/O pin Timer0_A, capture: CC10A input, compare: Out0 output ADC10 analog input A1 ⁽¹⁾
P1.2/ TA0.1/ A2	4	3	I/O	General-purpose digital I/O pin Timer0_A, capture: CC11A input, compare: Out1 output ADC10 analog input A2 ⁽¹⁾
P1.3/ ADC10CLK/ A3/ VREF-/VEREF	5	4	I/O	General-purpose digital I/O pin ADC10, conversion clock output ⁽¹⁾ ADC10 analog input A3 ⁽¹⁾ ADC10 negative reference voltage ⁽¹⁾
P1.4/ SMCLK/ A4/ VREF+/VEREF+/ TCK	6	5	I/O	General-purpose digital I/O pin SMCLK signal output ADC10 analog input A4 ⁽¹⁾ ADC10 positive reference voltage ⁽¹⁾ JTAG test clock, input terminal for device programming
P1.5/ TA0.0/ A5/ SCLK/ TMS	7	6	I/O	General-purpose digital I/O pin Timer0_A, compare: Out0 output ADC10 analog input A5 ⁽¹⁾ USI: clock input in I2C mode; clock input/output in SPI mode JTAG test mode select, input terminal for device programming
P1.6/ TA0.1/ A6/ SDO/ SCL/ TDI/TCLK	8	7	I/O	General-purpose digital I/O pin Timer0_A, capture: CC11A input, compare: Out1 output ADC10 analog input A6 ⁽¹⁾ USI: Data output in SPI mode USI: I2C clock in I2C mode JTAG test data input or test clock input during programming
P1.7/ A7/ SDI/ SDA/ TDO/TDI ⁽²⁾	9	8	I/O	General-purpose digital I/O pin ADC10 analog input A7 ⁽¹⁾ USI: Data input in SPI mode USI: I2C data in I2C mode JTAG test data output terminal or test data input during programming

ADC10 Registers

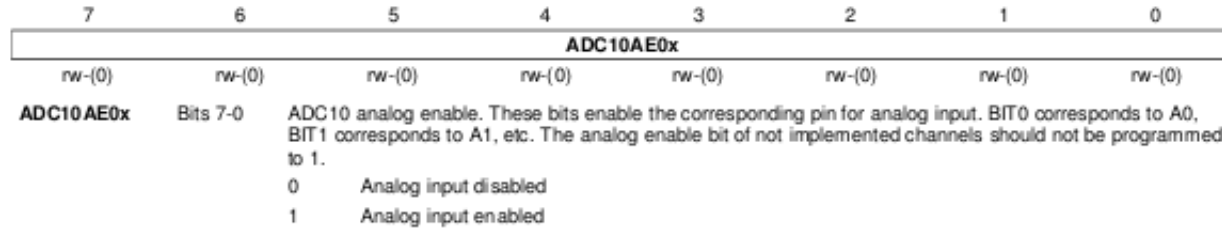
CONSEQx	Bits 2-1	Conversion sequence mode select
	00	Single-channel-single-conversion
	01	Sequence-of-channels
	10	Repeat-single-channel
	11	Repeat-sequence-of-channels
ADC10BUSY	Bit 0	ADC10 busy. This bit indicates an active sample or conversion operation
	0	No operation is active.
	1	A sequence, sample, or conversion is active.

DVSS	14	13, 14	NA	Ground reference
------	----	--------	----	------------------

```
ADC10AE0 |= 0x02;
```

```
// PA.1 ADC option select
```

22.3.3 ADC10AE0, Analog (Input) Enable Control Register 0



Using peripherals

```
#include "msp430.h"
```

```
void main(void)
```

```
{
```

```
    WDTCTL = WDTPW + WDTHOLD;
```

```
    // Stop WDT
```

```
    ADC10CTL0 = ADC10SHT_2 + ADC10ON;
```

```
    // ADC10ON
```

```
    ADC10CTL1 = INCH_1;
```

```
    // input A1
```

```
    ADC10AE0 |= 0x02;
```

```
    // PA.1 ADC option select
```

```
    P1DIR |= 0x01 ;
```

```
    // Set P1.0 to output direction
```

```
    for (;;)
    {
```

```
        ADC10CTL0 |= ENC + ADC10SC;
```

```
        // Sampling and conversion start
```

```
        while (ADC10CTL1 & ADC10BUSY);
```

```
        // ADC10BUSY?
```

```
        if (ADC10MEM < 0x2FF)
```

```
            P1OUT &= ~0x01;
```

```
        // Clear P1.0 LED off
```

```
        else
```

```
            P1OUT |= 0x01;
```

```
        // Set P1.0 LED on
```

```
    unsigned i;
```

```
    for (i = 0xFFFF; i > 0; i--);
```

```
    // Delay
```

```
    }
```

```
}
```

ADC10CTL0 = ADC10SHT_2 + ADC10ON;

// ADC10ON

22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
SREFx			ADC10SHTx		ADC10SR	REFOUT	REFBURST
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
MSC	REF2_5V	REFON	ADC10ON	ADC10IE	ADC10IFG	ENC	ADC10SC
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ENC = 0

SREFx	Bits 15-13	Select reference. 000 $V_{Rn} = V_{CC}$ and $V_{Rn} = V_{SS}$ 001 $V_{Rn} = V_{REF+}$ and $V_{Rn} = V_{SS}$ 010 $V_{Rn} = V_{REF+}$ and $V_{Rn} = V_{SS}$. Devices with V_{REF+} only. 011 $V_{Rn} = \text{Buffered } V_{REF+}$ and $V_{Rn} = V_{SS}$. Devices with V_{REF+} pin only. 100 $V_{Rn} = V_{CC}$ and $V_{Rn} = V_{REF-} / V_{REF+}$. Devices with V_{REF-} pin only. 101 $V_{Rn} = V_{REF+}$ and $V_{Rn} = V_{REF-} / V_{REF+}$. Devices with V_{REF+} pins only. 110 $V_{Rn} = V_{REF+}$ and $V_{Rn} = V_{REF-} / V_{REF+}$. Devices with V_{REF+} pins only. 111 $V_{Rn} = \text{Buffered } V_{REF+}$ and $V_{Rn} = V_{REF-} / V_{REF+}$. Devices with V_{REF+} pins only.
ADC10SHTx	Bits 12-11	ADC10 sample-and-hold time 00 4 × ADC10CLKs 01 8 × ADC10CLKs 10 16 × ADC10CLKs 11 64 × ADC10CLKs
ADC10SR	Bit 10	ADC10 sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate. Setting ADC10SR reduces the current consumption of the reference buffer. 0 Reference buffer supports up to ~200 kbps 1 Reference buffer supports up to ~50 kbps
REFOUT	Bit 9	Reference output 0 Reference output off 1 Reference output on. Devices with V_{REF+} / V_{REF-} pin only.
REFBURST	Bit 8	Reference burst. 0 Reference buffer on continuously 1 Reference buffer on only during sample-and-conversion
MSC	Bit 7	Multiple sample and conversion. Valid only for sequence or repeated modes. 0 The sampling requires a rising edge of the SHI signal to trigger each sample-and-conversion. 1 The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed
REF2_5V	Bit 6	Reference-generator voltage. REFON must also be set. 0 1.5 V 1 2.5 V
REFON	Bit 5	Reference generator on 0 Reference off 1 Reference on
ADC10ON	Bit 4	ADC10 on 0 ADC10 off 1 ADC10 on
ADC10IE	Bit 3	ADC10 interrupt enable 0 Interrupt disabled 1 Interrupt enabled

If the register descriptions don't have enough information then:

- 1) Look back earlier in the ADC10 chapter for more description of the operation.
- 2) Check the text book for an alternative
- 3) Ask a classmate or one of us!

ADC10IFG	Bit 2	ADC10 interrupt flag. This bit is set if ADC10MEM is loaded with a conversion result. It is automatically reset when the interrupt request is accepted, or it may be reset by software. When using the DTC this flag is set when a block of transfers is completed. 0 No interrupt pending 1 Interrupt pending
ENC	Bit 1	Enable conversion 0 ADC10 disabled 1 ADC10 enabled
ADC10SC	Bit 0	Start conversion. Software-controlled sample-and-conversion start. ADC10SC and ENC may be set together with one instruction. ADC10SC is reset automatically. 0 No sample-and-conversion start 1 Start sample-and-conversion

Lab 3/4, ADC:

```
ADC10CTL0 |= ENC + ADC10SC;  
while (ADC10CTL1 & ADC10BUSY);
```

```
while (a & b){
```

```
}
```

vs

```
while(a & b);
```

```
{
```

```
}
```